IS61WV5128EDBLL
IS64WV5128EDBLL

512K x 8 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM WITH ECC

NOVEMBER 2011

FEATURES

- High-speed access time: 8, 10 ns
- Low Active Power: 85 mW (typical)
- Low Standby Power: 7 mW (typical) CMOS standby
- Single power supply
  - — V_{DD} 2.4V to 3.6V (10 ns)
  - — V_{DD} 3.3V ± 10% (8 ns)
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available
- Error Detection and Error Correction

DESCRIPTION

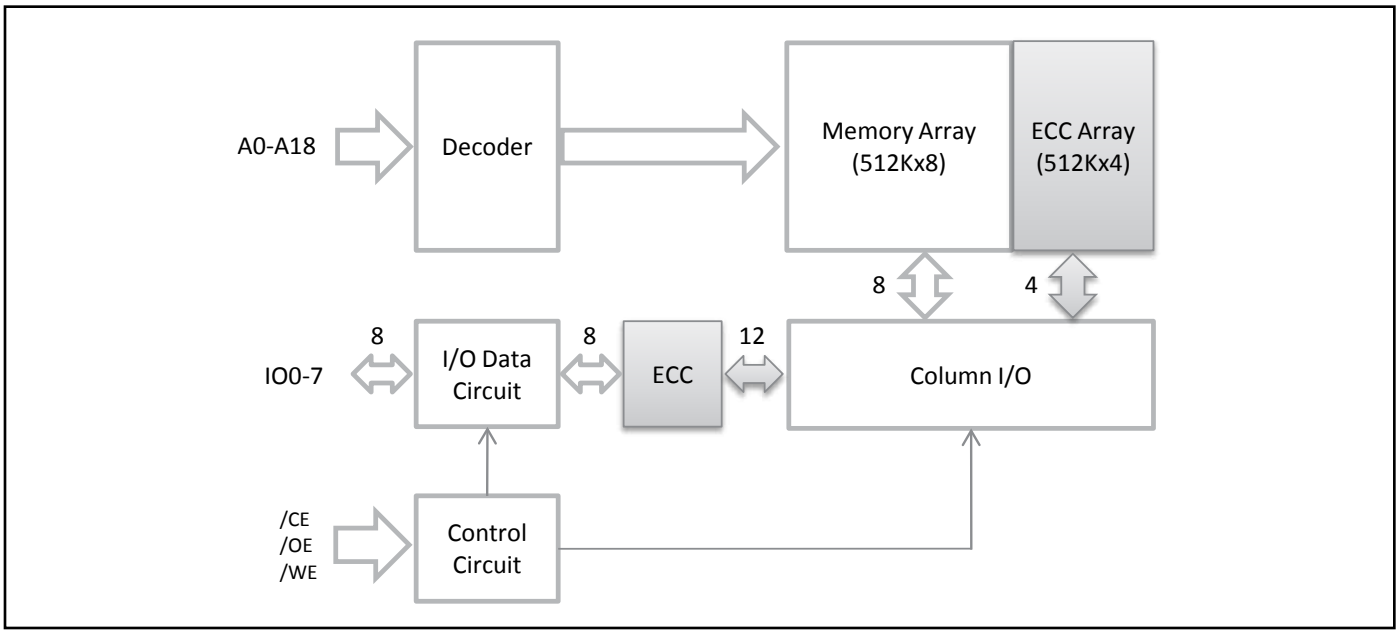
The *ISSI* IS61/64WV5128EDBLL is a high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

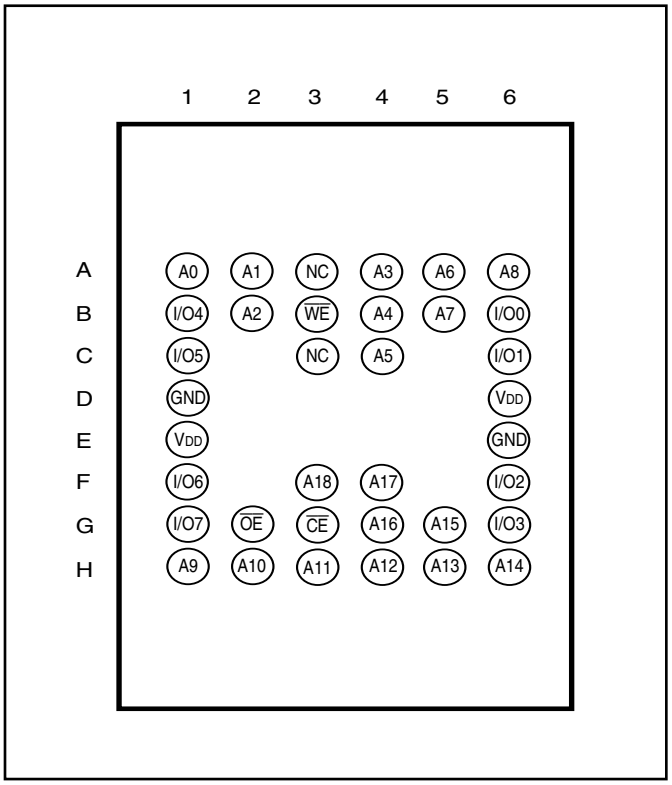
The IS61/64WV5128EDBLL is packaged in the JEDEC standard 44-pin TSOP-II, 36-pin SOJ and 36-pin Mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM

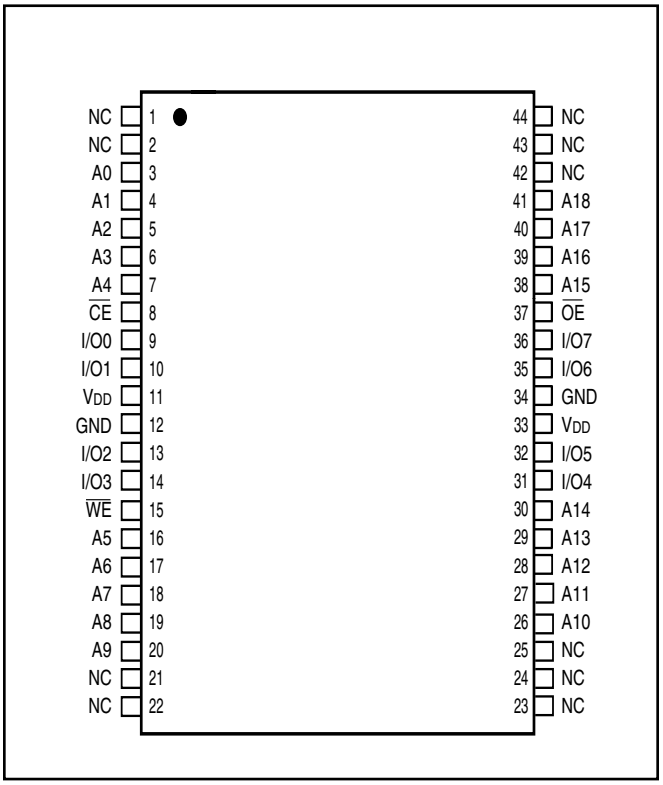


PIN CONFIGURATION (HIGH SPEED) (61/64WV5128ALL/BLL)

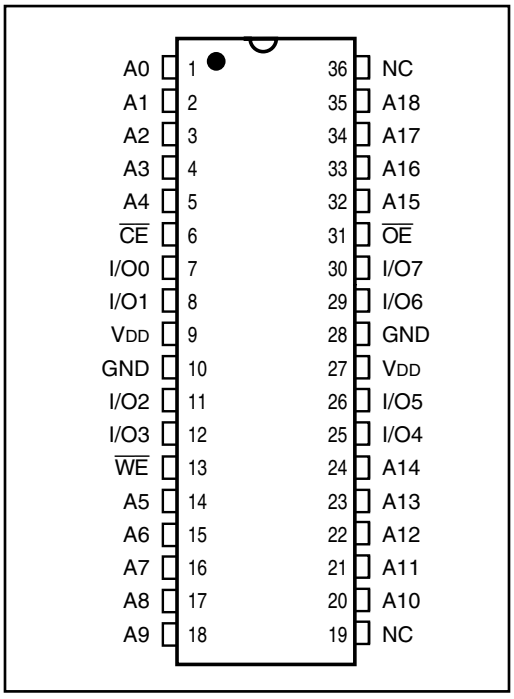
36 mini BGA



44-Pin TSOP (Type II)



36-Pin SOJ



PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V_{DD}	Power
GND	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{DD} + 0.5	V
V_{DD}	V_{DD} Relates to GND	–0.3 to 4.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC with hamming code for each byte
- Detect and correct one bit error per byte
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	H	X	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	L	H	H	High-Z	I_{CC}
Read	L	H	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

OPERATING RANGE (V_{DD})[1]

Range	Ambient Temperature	IS61WV5128EDBLL V_{DD} (8, 10ns)	IS64WV5128EDBLL V_{DD} (10ns)
Industrial	–40°C to +85°C	2.4V-3.6V (10ns) 3.3V ± 10% (8ns)	—
Automotive (A1)	–40°C to +85°C	—	2.4V-3.6V
Automotive (A3)	–40°C to +125°C	—	2.4V-3.6V

Note:
1. Contact SRAM@issi.com for 1.8V option

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V ± 10%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
   V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

				-8		-10		-20		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	40	—	30	—	25	mA
			Ind.	—	45	—	35	—	30	
			Auto.	—	—	—	50	—	45	
			typ.[2]	21		21				
I_{CC1}	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com.	—	20	—	20	—	20	mA
			Ind.	—	25	—	25	—	25	
			Auto.	—	—	—	40	—	40	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com.	—	10	—	10	—	10	mA
			Ind.	—	15	—	15	—	15	
			Auto.	—	—	—	30	—	30	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE}$ ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	5	—	5	—	5	mA
			Ind.	—	6	—	6	—	6	
			Auto.	—	—	—	15	—	15	
			typ.[2]	1.5		1.5				

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

AC TEST CONDITIONS

Parameter	Unit (2.4V-3.6V)
Input Pulse Level	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	1V/ ns
Input and Output Timing and Reference Level (V_{Ref})	V_{DD}/2
Output Load	See Figures 1 and 2

AC TEST LOADS

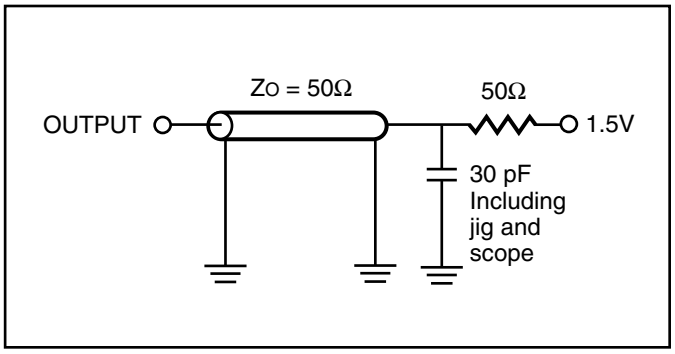


Figure 1.

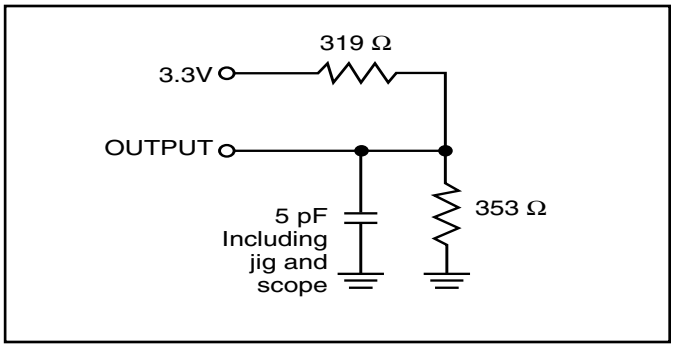


Figure 2.

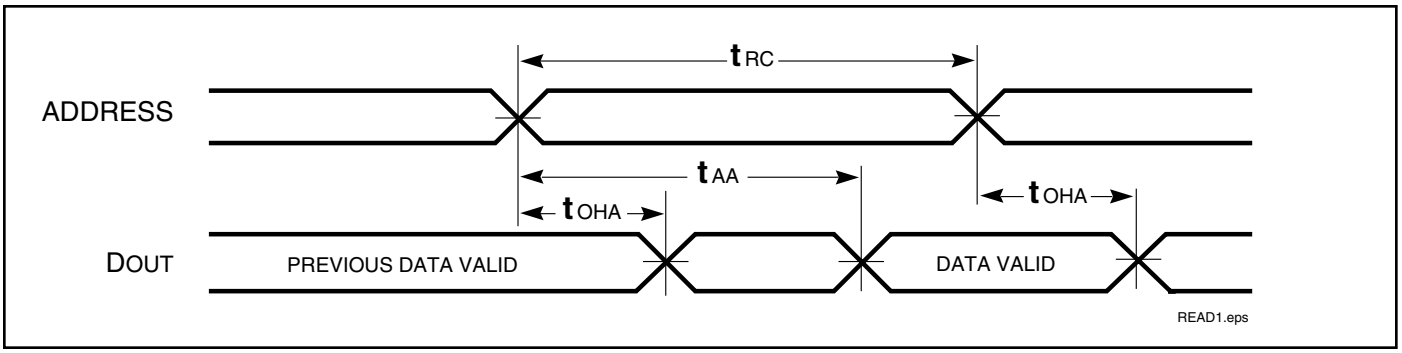
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-20 Min.	-20 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	20	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	20	ns
t_{OHA}	Output Hold Time	2.0	—	2.0	—	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4.5	—	4.5	—	8	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	3	—	4	—	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t_{HZCE}[2	$\overline{CE}$ to High-Z Output	0	3	0	4	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t_{PU}	Power Up Time	0	—	0	—	0	—	ns
t_{PD}	Power Down Time	—	8	—	10	—	20	ns

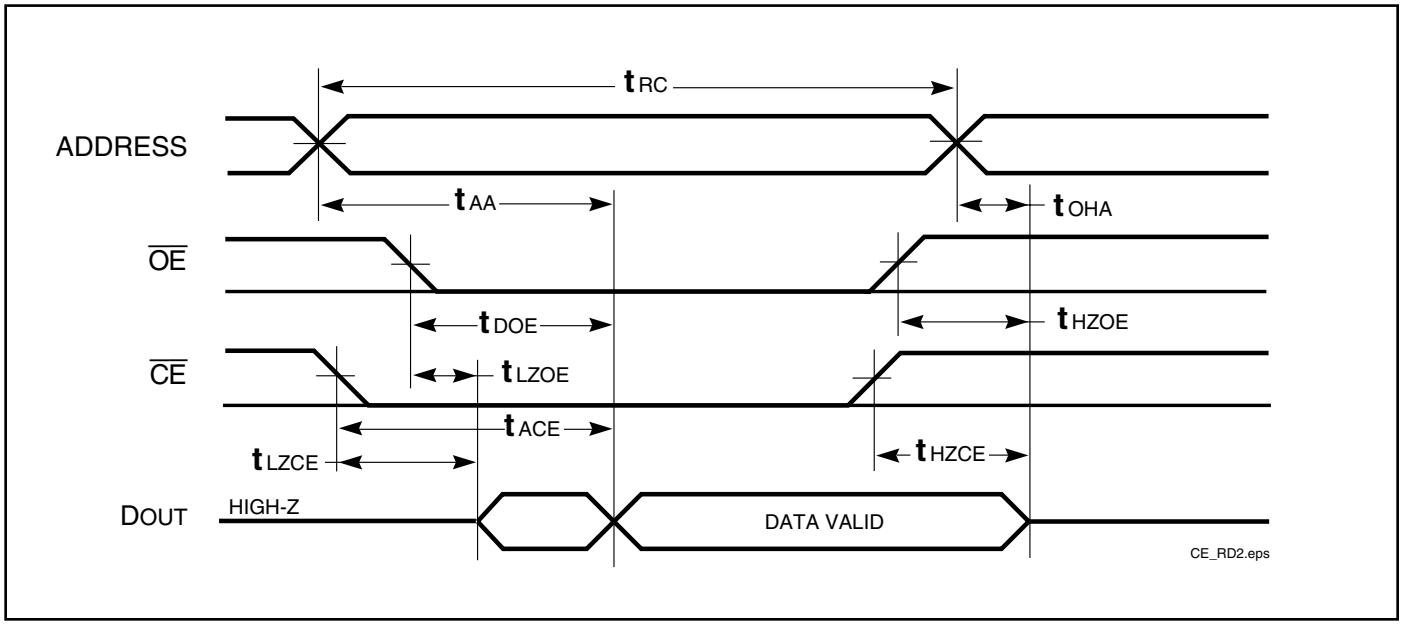
Notes:
1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = V_{IL})



READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

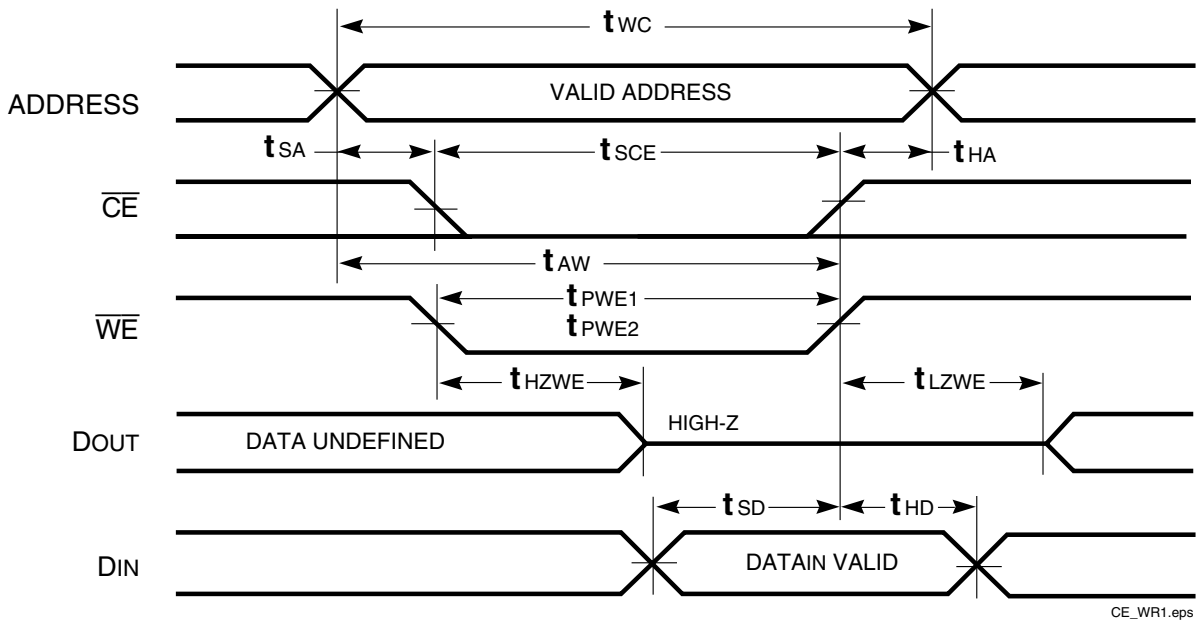
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	-20 Min.	-20 Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	12	—	ns
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	12	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	6.5	—	8	—	12	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8.0	—	10	—	17	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	9	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	—	9	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	2	—	ns

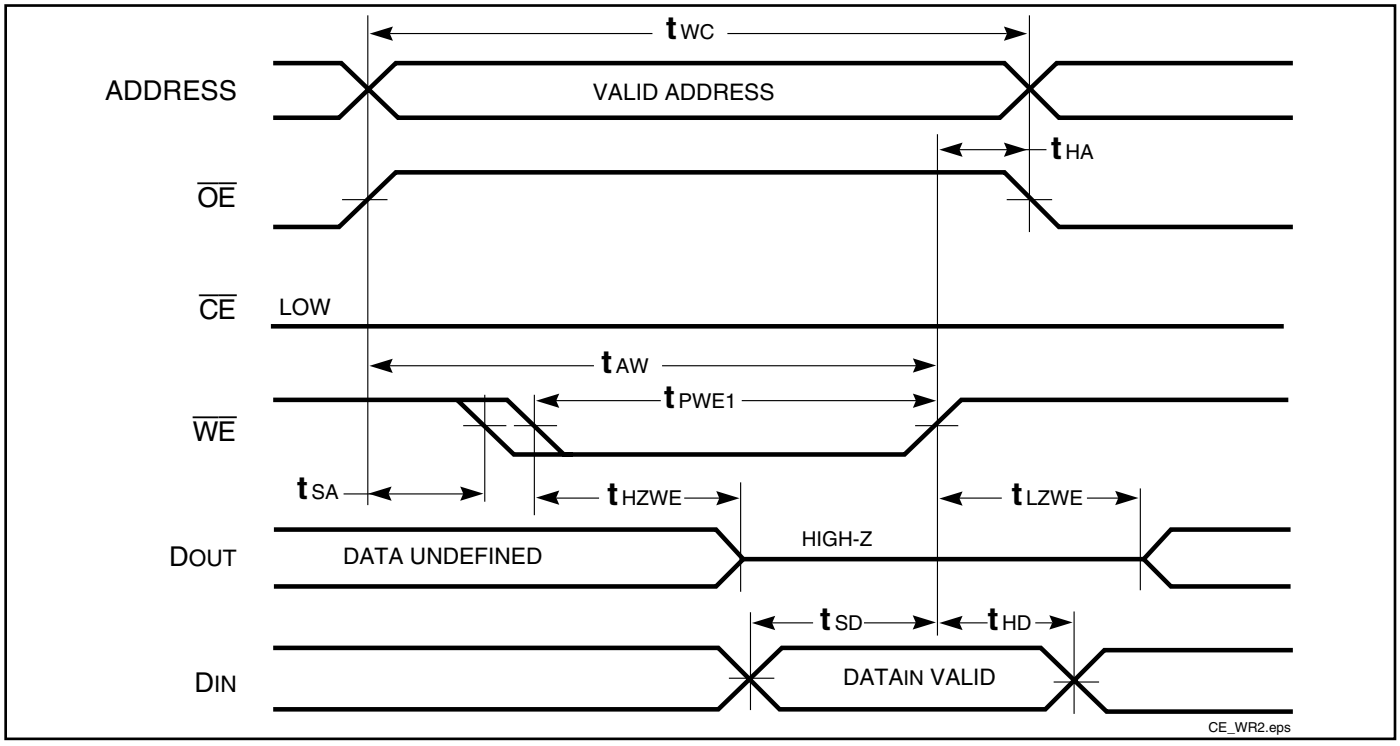
Notes:
1. Test conditions and output loading conditions are specified in the AC Test Conditions and AC Test Loads (Figure 1).
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

AC WAVEFORMS

WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)



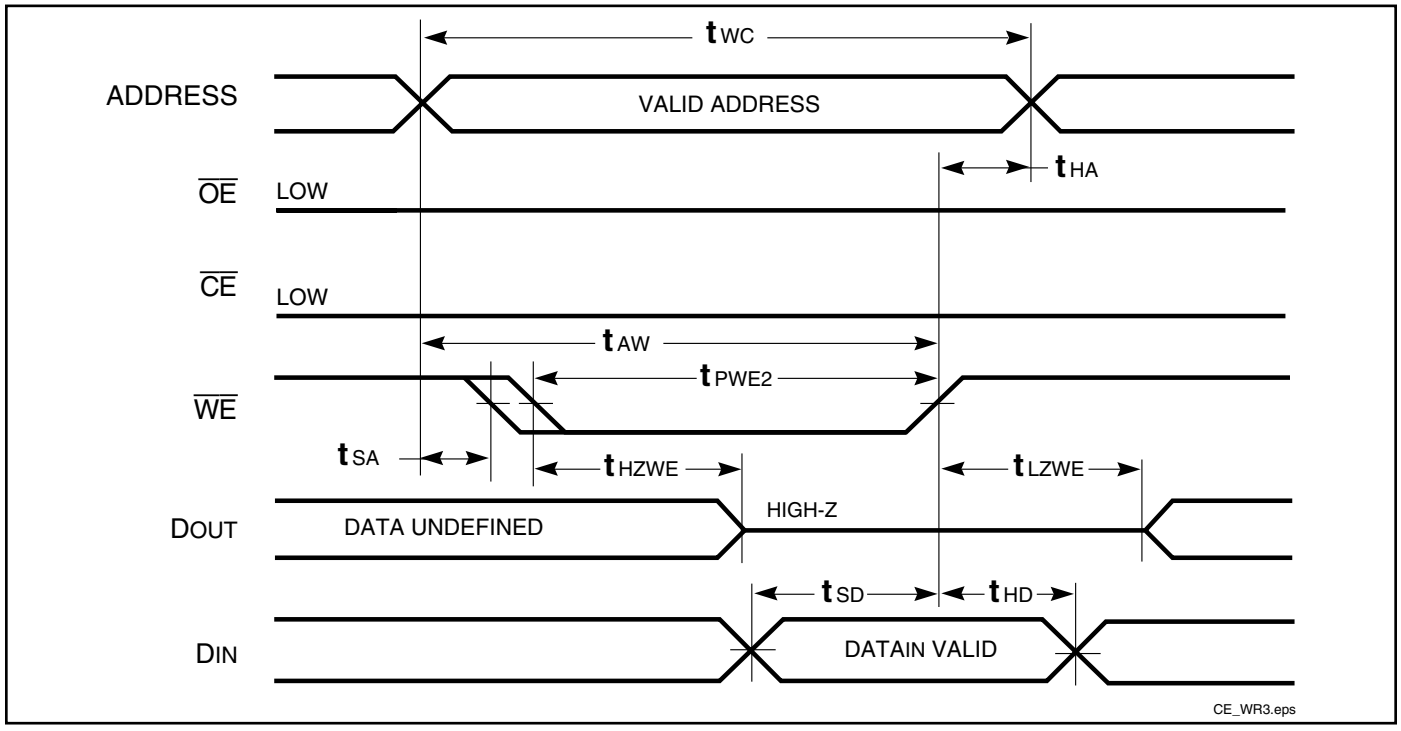
WRITE CYCLE NO. 2[1,2] ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ > V_{IH}.

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



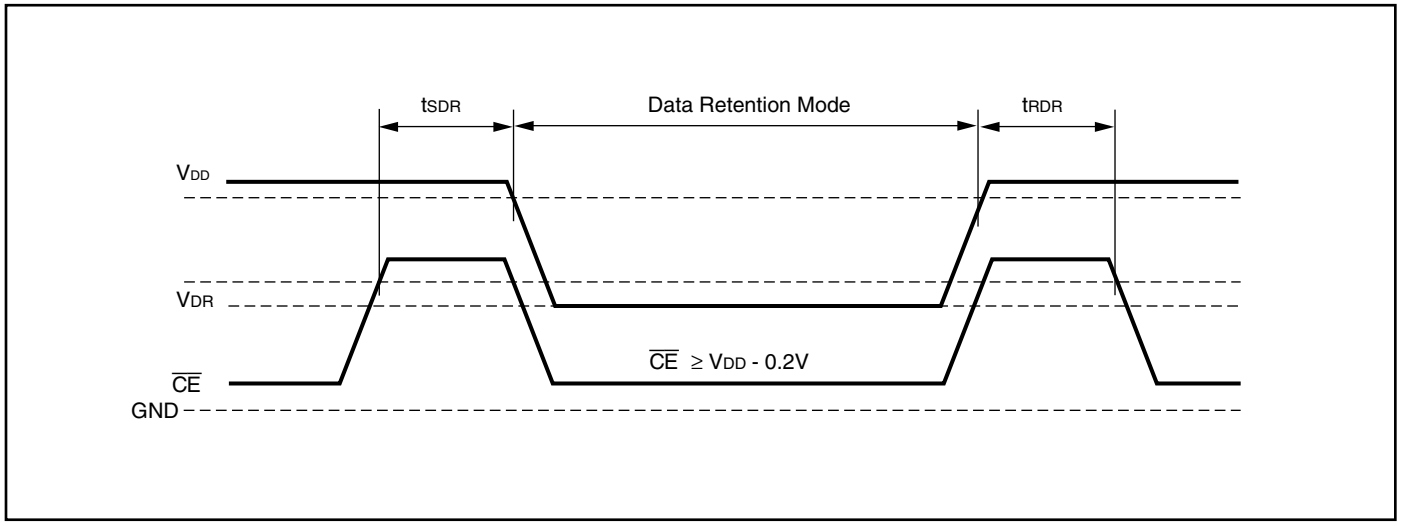
HIGH SPEED

DATA RETENTION SWITCHING CHARACTERISTICS (2.4V-3.6V)

Symbol	Parameter	Test Condition	Options	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	—	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	0.5	5	mA
			Ind.	—	—	6	
			Auto.			15	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	—	ns

Note 1: Typical values are measured at $V_{DD} = V_{DR}$(min), T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61WV5128EDBLL-10BI	36 mini BGA (6mm x 8mm)
	IS61WV5128EDBLL-10BLI	36 mini BGA (6mm x 8mm), Lead-free
	IS61WV5128EDBLL-10TI	TSOP (Type II)
	IS61WV5128EDBLL-10TLI	TSOP (Type II), Lead-free
	IS61WV5128EDBLL-10KLI	400-mil Plastic SOJ, Lead-free

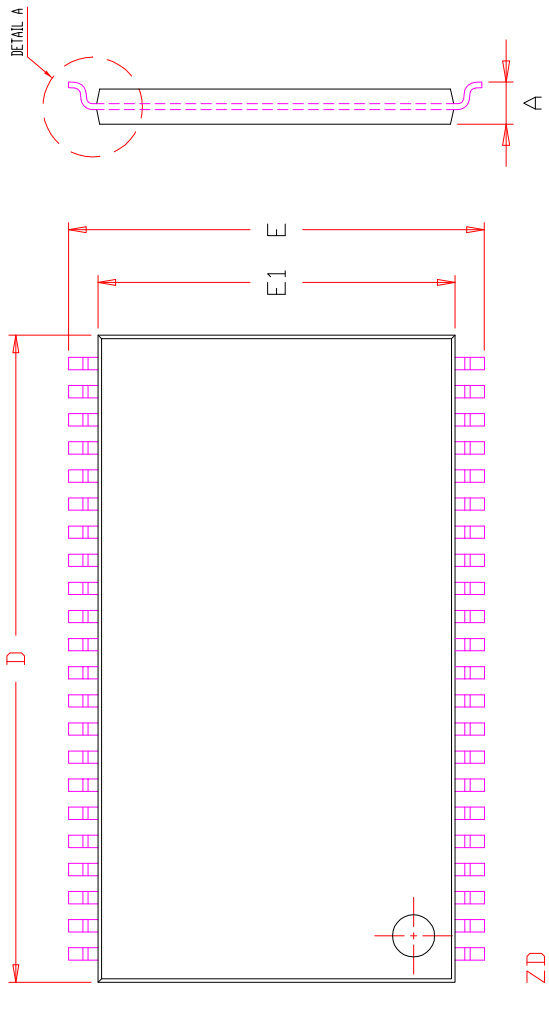
Automotive (A1) Range: -40°C to +85°C

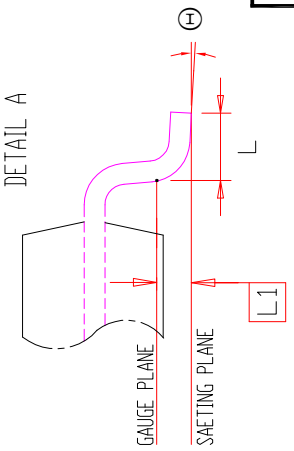
Speed (ns)	Order Part No.	Package
10	IS64WV5128EDBLL-10BA1	36 mini BGA (6mm x 8mm)
	IS64WV5128EDBLL-10BLA1	36 mini BGA (6mm x 8mm), Lead-free
	IS64WV5128EDBLL-10CTA1	TSOP (Type II), Copper Leadframe
	IS64WV5128EDBLL-10CTLA1	TSOP (Type II), Lead-free, Copper Leadframe
	IS64WV5128EDBLL-10KLA1	400-mil Plastic SOJ, Lead-free

Automotive (A3) Range: -40°C to +125°C

Speed (ns)	Order Part No.	Package
10	IS64WV5128EDBLL-10BA3	36 mini BGA (6mm x 8mm)
	IS64WV5128EDBLL-10BLA3	36 mini BGA (6mm x 8mm), Lead-free
	IS64WV5128EDBLL-10CTA3	TSOP (Type II), Copper Leadframe
	IS64WV5128EDBLL-10CTLA3	TSOP (Type II), Lead-free, Copper Leadframe
	IS64WV5128EDBLL-10KLA3	400-mil Plastic SOJ, Lead-free

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
θ	0	—	8°	0	—	8°

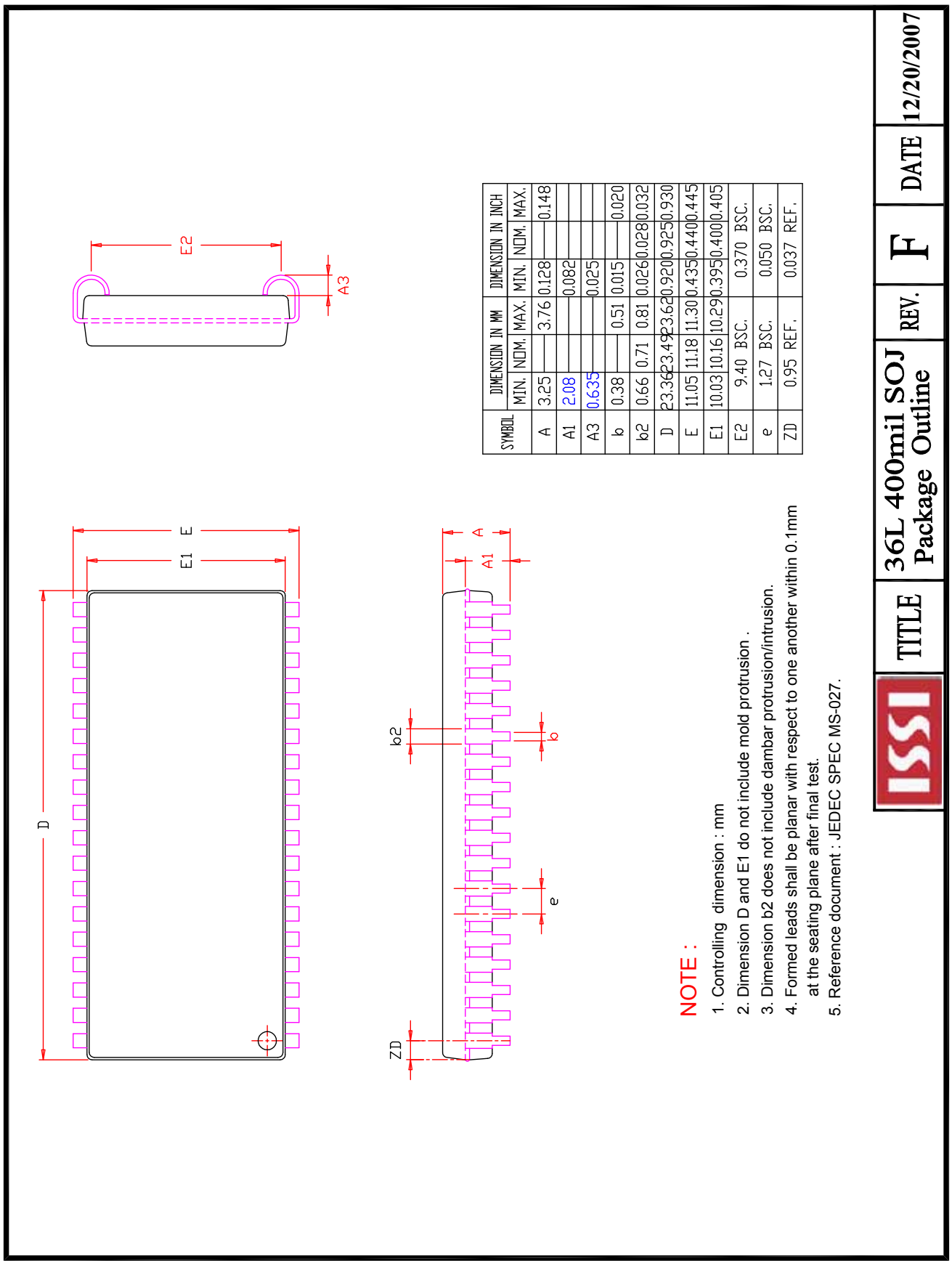




NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	REV.	DATE
ISSI	44L 400mil TSOP-2 Package Outline	F	06/04/2008

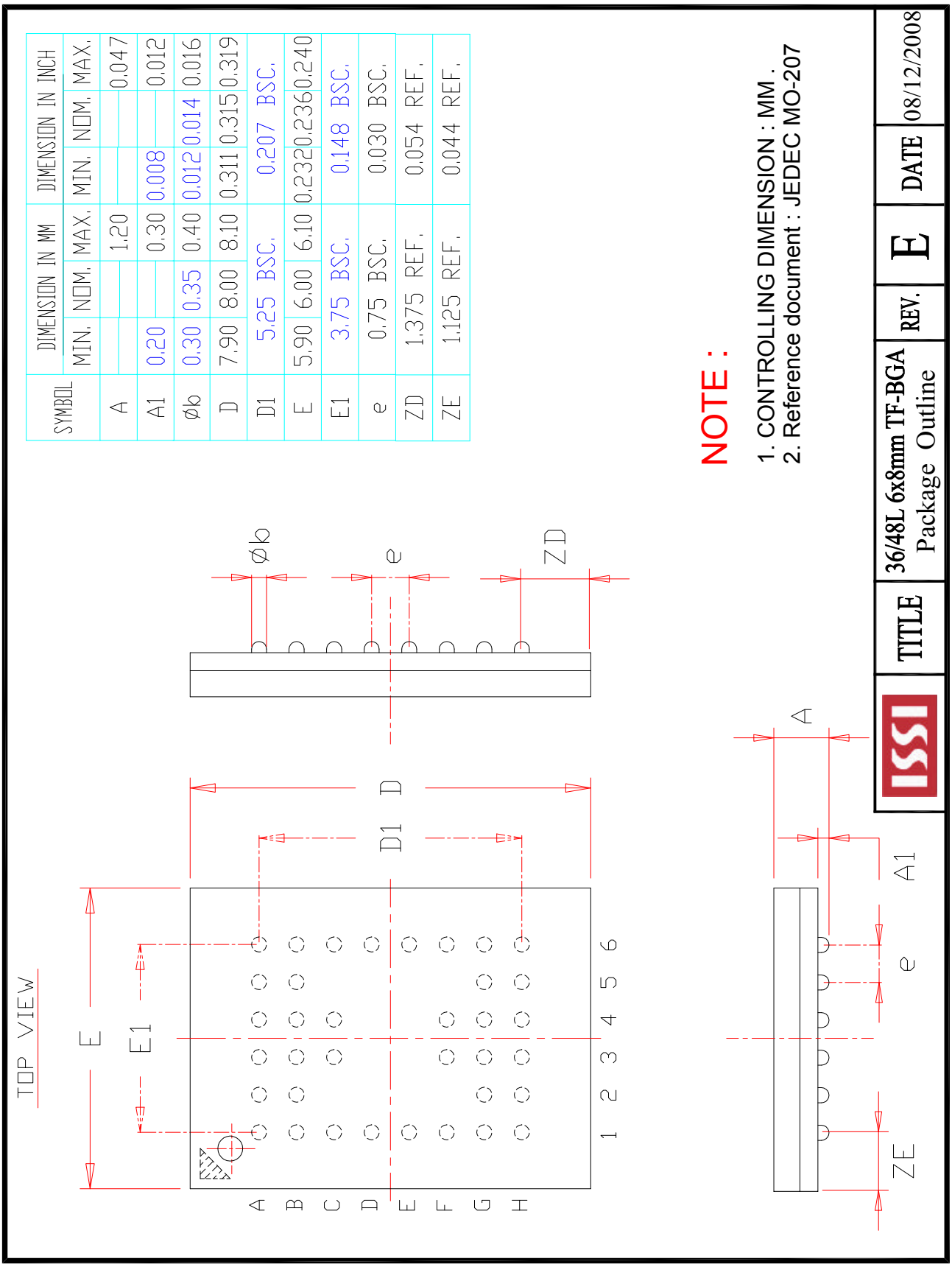


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	—	3.76	0.128	—	0.148
A1	2.08	—	—	0.082	—	—
A3	0.635	—	—	0.025	—	—
b	0.38	—	0.51	0.015	—	0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	23.36	23.49	23.62	0.920	0.925	0.930
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BSC.			0.370 BSC.		
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

	TITLE	36L 400mil SOJ Package Outline	REV.	F	DATE	12/20/2007


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
øb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC. 0.207 BSC.
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC. 0.148 BSC.
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
TOP VIEW
E
E1
D
D1
øb
e
ZD
A
A1
ZE
1 2 3 4 5 6
A B C D E F G H
ISSI
TITLE
36/48L 6x8mm TF-BGA
Package Outline
REV.
E
DATE
08/12/2008